In the Drawings

There are no amendments to the drawings.

Remarks

In response to the Examiner's Claim Objections, Applicant has amended Claims 25 and 34; and cancelled Claims 5, 6, 21, 22 and 27. Entry of the amendment and favorable consideration thereof is earnestly requested.

Claims 1 & 15

Claims 1 and 15 requires among other limitations a "camera control unit programmed based at least in part upon said timing signal particular to said camera head." Applicant respectfully submits that these limitations are not disclosed or taught in the cited prior art.

For example, U.S. Patent No. 6,046,769 ("Ikeda et al.") discloses that the image sensing apparatus is able to adapt to "changes of arrangement of the color filters and changes of the number of pixels of a CCD in the image sensing unit, by changing the application program loaded in a DSP without changing the hardware of the signal processor." (Col. 9, line 65 – Col. 10, line 2.) While the Examiner has pointed to this portion of the specification as supporting that the CCU is programmed based on the timing signal, Ikeda et al. does not disclose or teach this. Rather, Ikeda et al. teaches that "the bus controller 153 transmits a read request command for reading out CCD information to the image sensing controller 110" and that "after receiving the CCD information, the controller analyzes the CCD information . . . then outputs a request to the main CPU to load a signal processing program" and "the bus controller 153 controls

the DSP 201 to execute the loaded program." (Col. 8, lines 30-32, 43-46 & 60-61.) Therefore, the "DSP 201" is not programmed based on the timing signal, which the Examiner has identified as MCLK ("the timing signal actuating said imager and sent to said camera control unit (see Fig. 1 and note that MCLK is sent from 108 to 140)"). (Official Action 4/6/06, p. 5.)

It is well settled that "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). In this case, Applicant respectfully submits that Ikeda et al. fails to disclose a "camera control unit programmed based at least in part upon said timing signal particular to said camera head" as required by Claims 1 and 15 and therefore cannot anticipate Claims 1 and 15.

Claims 25 and 34

Claims 25 and 34 require "a serializer, for serializing the digital image signal." The Examiner has submitted that U.S. Patent No. 6,870,566 ("Koide et al.") discloses this limitation citing "FIFO memory 105." (*See*, Official Action 4/6/06, p. 6.) Applicant respectfully disagrees.

Koide et al. discloses that "[d]igital signals converted from analog signals by the A/D converter 103 are . . . temporarily stored in the FIFO memory 105" and that "as image signals are stored in the FIFO memory 105, the FIFO status flag 108 changes from F0 to F1, F1 to F2, and so on. When the FIFO status flag 108 indicates the state F1 . . . a predetermined amount of image signals are transmitted from the FIFO memory

105 through the interfaces 109 and 111, and stored in the memory 113 of the computer 12." (Col. 9, lines 64-67; Col. 10, lines.) Accordingly, while the Examiner has cited this memory as being a serializer, Applicant respectfully submits that FIFO memory merely acts as a temporary cache, in which, upon filling to certain levels, forwards the image signal to the computer. Nowhere does Koide et al. teach, disclose or suggest that the FIFO memory is or functions as a serializer for converting the data into a digital serial format for transmission and reception.

Accordingly, Applicant respectfully submits that because Koide et al. fails to teach, disclose or suggest a serializer, for serializing the digital image signal for transmission over said cable as required by Claims 25 and 34, Koide et al. cannot anticipate Claims 25 and 34.

Claim 1

Applicant has already argued above that Ikeda et al. fails to teach or suggest a "camera control unit programmed based at least in part upon said timing signal particular to said camera head" as required by Claim 1.

Applicant notes that the Examiner has submitted that "the timing signal actuating said image and sent to said camera control unit 140 (see Fig. 1 and note that VD, HD and MCLK are all sent to the controller 140)." (Official Action 4/6/06, p. 7.) However, Applicant notes that Ikeda et al. is not clear on this point, in fact, where Ikeda et al. does actually mention these signals, they are sent from the controller 140 to the image sensing unit 100, which is the opposite as suggested by the Examiner. (Col. 5, lines 60-67 "a timing signal generator 108 . . . generates various kinds of timing signals on the

basis of HD (horizontial synchronizing signal) and VD (vertical synchronizing signal) provided from the signal processing board 140 through the connector 111.") While the Examiner further states that MCLK is sent to the controller, Ikeda et al. is actually silent on this point. (Official Action 4/6/06, pp. 5 & 7.) Therefore, Ikeda et al. actually teaches that the bus controller controls the signal processing unit (or DSP), which sends timing and synchronizing signals to the timing generator for control of the timing generator, not the other way around. (*See*, FIGS. 1, 2 & 4; Col. 6, line 63 – Col. 7, line 4.)

The Examiner further goes on to submit that Ikeda et al. teaches that the camera control unit is programmed by the timing signal. (Official Action 4/6/06, p. 8.) Applicant disagrees as noted above in connection with the arguments for Claim 15. However, in addition, Applicant notes that the Examiner has suggested combining Ikeda et al. with Koide et al. in rejecting Claim 1.

Koide et al. is clear that the camera control unit is not programmed by the timing signal, but fully controls the timing generator. For example, Koide et al. teaches that "the computer supervises the FIFO status flag . . . as image signals are stored in the FIFO memory 105, the FIFO status flag 108 changes from F0 to F1, F1 to F2" and "[w]hen the FIFO status flag 108 indicates the state F1 . . . the process proceeds to step S34 where a predetermined amount of image signals are transmitted from the FIFO memory." (Col. 10, lines 36-43.) Koide et al. further states that "the FIFO status flag 108 is checked . . . and if it indicates the state F2, which shows that the rate of the computer 12 for receiving the image signals from the image sensing unit 11 is lower than the rate of the image sensing operation, the computer issues an instruction to the

control unit 107 to control the TG 106 to lower the rate of generating timing pulses." (Col. 10, lines 46-54.) Therefore, while the Examiner has provided one explanation with respect to how Ikeda et al. may or may not work, Koide et al. clearly states that the camera control unit controls the timing generator.

It is well settled that the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *See, e.g.,* MPEP 2143.01; *In re Mills*, 916 F.2d 680, 682, 16 USPQ2d 1430, 1432 (Fed. Cir. 1990) (fact that prior art "may be capable of being modified to run the way the apparatus is claimed, there must be some suggestion or motivation in the reference to do so."). In the present case, Applicant respectfully submits that Ikeda et al. does not teach that the camera is programmed based on the timing signal, but rather on a program accessed by the computer. (Col. 8, lines 30-32, 43-46 & 60-61.) In addition, Koide et al. teaches that the computer controls the timing generator. (Col. 10, lines 46-54.) Accordingly, there is no suggestion in either reference that the camera control unit is programmed based on the timing signal, but in fact, both references directly teach away from this limitation.

Accordingly, Applicant respectfully submits that Ikeda et al. and Koide et al. are not properly combinable as the Examiner has suggested as Koide et al. teaches away from the proposed modification of Ikeda et al. and therefore cannot render Claim 1 obvious.

The Examiner further submits that Ikeda et al. teaches "a serializer (note that although a serializer is not shown the image signal must necessarily be serialized as the

cable is described as a "serial communication line," see Column 7 lines 46-47, and the entirety of the image data can not be sent at once over a single line and therefore there must be a serializer for serializing the image signal), for serializing the image signal for transmission over said cable." (Official Action 4/6/06, pp. 7-8.)

First, Applicant notes that, as the Examiner is aware, all limitations of all claims must be considered, because it is improper to fail to consider any limitation in the claims. *In re Geerdes*, 491 F.2d 1260, 1262, 180 U.S.P.Q. 789, the 791 (CCPA 1974). In this case, Claim 1 requires "a serializer, for serializing the digital image signal for transmission." (emphasis added.) The Examiner has cited to a portion of the specification of Ikeda et al. referring to the transmission of command signals, not image signals. (See, Col. 7, lines 43-49 "command for zooming and focusing, the bus controller 153 sends the command to the image sensing unit 100 via the connector 150 through the serial communication line.") With regard to the image signal, Ikeda et al. teaches that an analog signal is sent from the CCD 13 to the sample and hold / automatic gain control 104 through a shielded cable to an A/D converter in 140. (*See*, FIGS. 1, 2, 4 and 5; Col. 5, lines 52-59 & Col. 6, lines 18-26.) Nowhere does Ikeda et al. teach, disclose or suggest a serializer, for serializing the digital image signal for transmission, but in fact, teaches away from this limitation as the image signal transmitted is an analog signal, not a serialized digital signal.

Accordingly, Applicant respectfully submits that, while Ikeda et al. and Koide et al. are not properly combinable, even if they were combined, one would not arrive at the

pending claims as neither reference teaches or suggests a serializer, for serializing the digital image signal for transmission as required by Claim 1.

It is respectfully submitted that claims 1 – 41, all of the claims remaining in the application, are in order for allowance and early notice to that effect is respectfully requested.

Respectfully submitted,

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Wesley W. Whitmyer, Jr., Registration No. 33,558
Steven B. Simonis, Registration No. 54,449
Attorneys for Applicants
ST. ONGE STEWARD JOHNSTON & REENS LLC
986 Bedford Street
Stamford, CT 06905-5619
203 324-6155